WHAT IS CLAIMED IS:

1. A wireless peak-to-average reduction circuit for use with multi-carrier power amplifiers in a wireless communication system to enhance the linearity and performance of the amplifier, in particular wireless cellular, PCS, wireless LAN, line of sight microwave, military, and satellite communication systems and any other none wireless applications, the peak-to-average reduction circuit comprising:

   - A multi-carrier receiver for the peak-to-average reduction of IF or RF input signal to amplifier. If the input signal is baseband then the multi-carrier receiver is bypassed.

   - A digital signal processing block to peak-to-average reduce the multi-carrier input signal using lookup table.

   - A digital signal processing block to use the input and the output of the peak-to-average reduction to produce the phase rotation lookup table.

   - A digital signal processing block to converts the multi-carrier baseband input signal to individual carrier base band signals. The individual carrier baseband signal is first amplitude limited and then phase rotated before being up converted to its original multi-carrier baseband signal.

   - A digital signal processing block that clips the amplitude of the individual carrier baseband signal by preserving the phase.

   - A multi-carrier transmitter block that prepare the peak-to-average reduced multi-carrier signal for delivery to multi-carrier power amplifier.

2. The peak-to-average reduction circuit according to claim 1, wherein main multi-carrier input signal from the wireless transmitter is sampled using sub-harmonic sampling technique at the input frequency or at an intermediate frequency.

3. The peak-to-average reduction circuit according to claim 1, wherein the multi-carrier input signal from the wireless transmitter is sampled using sub-harmonic sampling technique at the input frequency or at an intermediate frequency and the digitized main multi-carrier input signal is down converted digitally and decimated to the appropriate number of samples per symbol for further digital signal processing.

4. The peak-to-average reduction circuit according to claim 1, wherein the multi-carrier input signal from the wireless transmitter is baseband and is sampled using Nyquist sampling technique and interpolated to produce the baseband multi-carrier signal with appropriate number of samples per symbol.

5. The peak-to-average reduction circuit according to claim 1, wherein the multi-carrier input signals from the wireless transmitter are in bit domain and the bit domain baseband signals are up converted, combined and interpolated to produce the digital multi-carrier baseband signal with appropriate number of sample per symbol.

6. The peak-to-average reduction according to claim 1, wherein the digital multi-carrier baseband signal is converted to single channel baseband signals by digital down conversion. The individual baseband signals are amplitude limited and phase rotated using the phase from phase rotation lookup table, then filtered and up converted back to their original baseband frequency before all individual baseband signals being combined again to produce the multi-carrier peak-to-average reduced baseband signal.

7. The peak-to-average reduction according to claim 1, wherein the digital multi-carrier baseband signal is converted to single channel baseband signals by

digital down conversion. The individual baseband signals are amplitude limited by a clipping circuit that calculates the amplitude and phase of the baseband signal. The amplitude of the baseband signal is clipped or is amplitude limited and then using the phase converted back to complex baseband signal.

8. The peak-to-average reduction circuit according to claim 1, wherein the peak-to-average reduced signal is digitally up converted and converted to analog domain at an intermediate frequency or the output frequency.

9. The peak-to-average reduction circuit according to claim 1, wherein the peak-to-average reduction phase rotation lookup table is created using the input and the output from the peak-to-average reduction block during the calibration.

10. The peak-to-average reduction circuit according to claim 1, wherein the received signal strength of the input signal to peak-to-average reduction circuit and transmit signal strength of the output from the peak-to-average reduction circuit is dynamically measures to adjust the total gain of the peak-to-average reduction circuit zero

11. The peak-to-average reduction circuit according to claim 1 and subsequent claims, when it is used in wireless cellular, wireless PCS, wireless LAN, microwave, wireless satellite, none wireless amplifiers, and any wireless communication systems used for military applications.

12. The peak-to-average reduction circuit according to claim 1, wherein the DSP function can be implemented in programmable logic, FPGA, Gate Array, ASIC, and DSP processor